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(54) PRODUCTION OF BUMP

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method for producing a bump exhibiting high reliability and durability after flip-chip mounting in which contact resistance is decreased by cleaning the surface of a finished bump.
SOLUTION: After ball bumps 8 are formed through a specified processa semiconductor substrate 1 is subjected to sputter etching in Ar gas atmosphere in order to remove an impurity layer 9 from the surface of the ball bump 8 thus exposing the clean surface thereof. Uppermost surface of polyimide 3 is then activated by ion impact. Sputter etching may be carried out in an atmosphere containing a reducing gas. Alternativelythe semiconductor substrate 1 may be subjected to ashing in an atmosphere containing oxygen after forming the ball bumps 8 and then subjected to sputter etching in an inert atmosphere or an atmosphere containing at least a reducing gas.

CLAIMS

[Claim(s)]
[Claim 1]A vamp manufacturing method having the process of performing sputter etching processing in an inert gas atmosphereto a base after bump formation.
[Claim 2]The vamp manufacturing method according to claim 1wherein the

above-mentioned vamp is a solder ball bump.
[Claim 3]The vamp manufacturing method according to claim 1 performing the above-mentioned sputter etching processing controlling independently a plasma discharge output and bias voltage to the above-mentioned base at least.
[Claim 4]The vamp manufacturing method according to claim 1 more than 1x10 $^{11}cm^{-3}$ performing the above-mentioned sputter etching processing with plasma density of less than 1x10 $^{14}cm^{-3}$.
[Claim 5]A vamp manufacturing method having the process of performing sputter etching processing in atmosphere which contains reducing gas at leastto a base after bump formation.
[Claim 6]The vamp manufacturing method according to claim 5wherein the above-mentioned vamp is a solder ball bump.
[Claim 7]The vamp manufacturing method according to claim 5 performing the above-mentioned sputter etching processing controlling independently a plasma discharge output and bias voltage to the above-mentioned base at least.
[Claim 8]The vamp manufacturing method according to claim 5 more than 1x10 $^{11}cm^{-3}$ performing the above-mentioned sputter etching processing with plasma density of less than 1x10 $^{14}cm^{-3}$.
[Claim 9]A vamp manufacturing method having the process of performing sputter etching processing continuously in an inert gas atmosphere or atmosphere which contains reducing gas at least after performing ashing treatment to a base after bump formation in atmosphere which contains oxygen at least.
[Claim 10]The vamp manufacturing method according to claim 9wherein the above-mentioned vamp is a solder ball bump.
[Claim 11]The vamp manufacturing method according to claim 9 performing the above-mentioned ASSHINNGU processing and/or the above-mentioned sputter etching processing controlling independently a plasma discharge output and bias voltage to the above-mentioned base at least.
[Claim 12]The vamp manufacturing method according to claim 9 more than 1x10 $^{11}cm^{-3}$ performing the above-mentioned ashing treatment and/or the above-mentioned sputter etching processing with plasma density of less than 1x10 $^{14}cm^{-3}$.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]

[Field of the Invention]Especially this invention avoids poor generating resulting from residuecontaminationetc. in a wetback process about a vamp manufacturing methodand relates to the vamp manufacturing method for realizing improvement in adhesion with the contact resistance of a vampa surface-protection filmand sealing resin.
[0002]
[Description of the Prior Art]In order to develop the miniaturization of electronic equipment furtherit is an important point how component-mounting density is raised. things -- development of high-density-assembly artsuch as a flip-chip-mounting method which mounts a bare chip to an immediate printing wiring boardis briskly performed as substitution of the conventional package mounting also about mounting of an integrated circuit (IC) and large scale integration circuit (LSI).
[0003]One of the PURIPPU chip mounting method of this has a method of mounting the thing in which the solder ball bump was formed on the aluminum (aluminum) electrode pad of an IC chip or an LSI chip in a printed-circuit board. Although there is a method using the electrolytic plating method as a method of forming this solder ball bump on a predetermined Al electrode padIn this casein order that the thickness of the solder film formed may receive the influence by dispersion with slight surface state of a ground and electrical resistanceit is fundamentally difficult for height to form the uniformly equal solder ball bump within an IC chip.
[0004]Thenthe method of forming a solder ball bump from before as a method of controlling dispersion in the height of a solder ball bump using membrane formation of the solder film by a vacuum deposition method and the lift off of a resist pattern is known. An example of the formation process of the solder ball bump by this method is explained belowreferring to drawing 6.
[0005]Namelyin the manufacturing method of this conventional solder ball bumpFirstas shown in drawing 6 Asputtering process and the dry etching method are used for the prescribed position on the semiconductor base substances 101such as a silicon (Si) wafer in which the circuit element etc. were formedand Al electrode pad 102 of specified shape is formed in it. Nextan opening is formed in the portion corresponding to the Al electrode pad 102 top of this passivation film after forming a passivation film (not shown) like a silicon nitride (SiN) film all over the semiconductor base substance 101for example. Nextan opening is formed in the portion corresponding to the Al electrode pad 102 top of this polyimide film 103 after forming a polyimide film on this passivation filmfor example.

[0006]Nextafter laminating a chromium (Cr) filma copper (Cu) filmand a golden (Au) film on the whole surface one by onefor example and forming Cr/Cu/Au membrane in it by sputtering processThe BLM (BallLimiting Metal) film 104 which consists of this patterned Cr/Cu/Au membrane is formed by patterning mostly this Cr/Cu/Au membrane after Al electrode pad 102 and identical shape. This BLM film 104 also has a role of a barrier metal of the solder ball bump formed behind.
[0007]Nextas shown in drawing 6 Bafter forming a resist film the whole surface on the semiconductor base substance 101this resist film is patterned after specified shape by the lithography method. The numerals 105 show the resist pattern of the specified shape formed of this. This resist pattern 105 has the opening 106 of a predetermined size into the portion corresponding to the BLM film 104 toptherefore the portion corresponding to the Al electrode pad 102 top.
[0008]Nextas shown in drawing 6 Cafter forming the solder film 107 in the whole surface with a vacuum deposition methodas shown in drawing 6 Dthe resist film 105 is removed with the solder film 107 on it by the lift-off method. Therebythe garbage of the solder film 107 is removed and the solder film 107 is patterned after desired shape. Thenby heat-treating and carrying out melting of the solder film 107as eventually shown in drawing 6 Ethe almost spherical solder ball bump 108 is formed.
[0009]Herethe process of rounding off the solder film 107 spherically by heat treatment shown in drawing 6 E is usually called a wetback. Supposing the natural oxidation film is thickly formed in the surface of the solder film 107even if it will heat-treatmelting of solder will not progress uniformly but it will become impossible to form the solder ball bump 108 well in this wetback's process.
[0010]Thereforeafter usually patterning the solder film 107 by a lift offFlux which has a reducing action and a surface activity operation beforehand all over the semiconductor base substance 101 before performing a wetback process (the main ingredients) By coating uniformly resinous principlessuch as an amine system active agentan alcohol solventrosinand the PORIGURI goaland performing heat treatment from the state. Formation of the solder ball bump 108 promoted and stabilized [that solder is spherically round with melting and surface tension of solder and] is realized.
[0011]
[Problem(s) to be Solved by the Invention]Although organic chemical washing is performed in the manufacturing method of the above-mentioned conventional solder ball bump to the semiconductor base substance 101 (refer to drawing 6 E) after the solder ball bump 108 was formed by heat

treatment and flux is washed outIf the organic component in flux carbonized during heat treatmentand it has stuck to the wafer surface at this time or the cleaning method of flux is unsuitableIt may remain in the surface of the solder ball bump 108or its neighborhood as residuewithout the ability to remove even after the solid content in flux washing. If the storage state after formation of the solder ball bump 108 is unsuitable and oxidation of the solder ball bump 108 progressesa natural oxidation film may be formed in the surface. The numerals 109 show impurity filmssuch as a contaminant which adhered in the wetback processand a natural oxidation film of the surface of the solder ball bump 108among drawing 6 E. Herethe impurity layer 109 of the surface of the expedient top of expression and the solder ball bump 108 was exaggeratedand the twist is also actually written thickly.
[0012]Thusif the impurity layer 109 exists in the surface of the solder ball bump 108as shown in drawing 7When applying the probe 110 to the surface of the solder ball bump 108and measuring an electrical propertyand the impurity layer 109 intervenes among bothcontact resistance becomes large and will cause the fault of it becoming impossible to perform exact evaluation etc. In such the statewhen flip chip mounting is carried outcontact resistance with a printed-circuit board will also increase.
[0013]Although **** is a problem in case the impurity layer 109 exists in the surface of the solder ball bump 108the residue thing resulting from a processcontaminationetc. will remain actually also on the polyimide film 103 which is the outermost surface of the chip in which the solder ball bump 108 was formed. When flip chip mounting of the chip of this state is carried out on a printed-circuit boardthe adhesion strength between the polyimide film 103 and sealing resin becomes weakand originates in itIt leads also to a crack occurring in the solder ball bump 108and bonding strength deteriorating or causing the fall of a reliability life by the rise of connection resistance.
[0014]Thereforethere is the purpose of this invention in providing the vamp manufacturing method which has high reliability and endurance after flip chip mounting while it defecates the surface of the vamp after a result and aims at reduction of contact resistance.
[0015]
[Means for Solving the Problem]To achieve the above objectsa vamp manufacturing method by the 1st invention in this invention has the process of performing sputter etching processing which used inactive gas after bump formation.
[0016]A vamp manufacturing method by the 2nd invention in this invention

has the process of performing sputter etching processing after bump formation in atmosphere which contains reducing gas at least.
[0017]A vamp manufacturing method by invention of the 3rd of this invention has the process of performing sputter etching processing continuously in inactive gas or atmosphere which contains reducing gas at leastafter performing ashing treatment after bump formation in atmosphere which contains oxygen at least.
[0018]In a typical embodiment of this inventiona vamp is a solder ball bump.
[0019]Sputter etching processing is performed in a suitable embodiment of this inventioncontrolling independently a plasma discharge output and bias voltage to a base. A plasma treatment apparatus which has two independently controllable RF generators is used for sputter etching processing in this case in a plasma discharge output and bias voltage at least.
[0020]In other suitable embodiments of this inventionmore than $1x10^{11}cm^{-3}$ performs sputter etching processing with plasma density of less than $1x10^{14}cm^{-3}$. In sputter etching processing in this casea source of ICP (Inductively Coupled Plasma)A plasma treatment apparatus which has sources of high density plasmasuch as a source of TCP (Transfer Coupled Plasma)an ECR (Electron Cyclotron Resonance) plasma sourceor a source of helicon wave plasmais used.
[0021]Since it has the process of performing sputter etching processing in inert gas atmospheressuch as Ar gasto a base after bump formation according to the 1st invention by this invention constituted as mentioned aboveThe surface of a pure vamp can be exposed by removing a natural oxidation film and process residue which were formed on the surface of a vamp. By thiscontact resistance with a probe at the time of measuring electrical resistance and contact resistance with a printed-circuit board after flip chip mounting can be reduced by the surface of a vamp after a result being defecated. While the electrical property of a device which produced a vamp is improved as for these resultsreliability and endurance of a product assembled by carrying out flip chip mounting of this device can be substantially raised compared with the former.
[0022]According to the 2nd invention in this inventiona vamp which has higher reliability than the 1st invention can be formed. Like a case of the 1st inventionalthough sputter etching processing is performed to a base after bump formationspecificallysputter etching processing is performed not in inactive gas but in atmosphere which contains reducing gassuch as hydrogen fluoride (HF)at least in that case. Since sputter

etching advances returning a natural oxidation film of the surface of a vamp formed at a wetback's process by this by originating in oxygen and moisture which are incorporated into a vampthe surface of a vamp can be cleaned more effectively than the 1st invention.
[0023]Thuscontact resistance with a probe or a printed-circuit board can be further reduced by the surface of a vamp after a result being defecated more effectively. As a resultwhile the electrical property of a device which produced a vamp is improved substantiallyreliability and endurance of a product assembled by carrying out flip chip mounting of this device can be raised more than the 1st invention.
[0024]According to the 3rd invention in this inventiontwo steps of plasma treatment are performed to a base after bump formation. Plasma treatment is performed in oxygen gas atmosphereit is the process reason of a wetback process or a resist processandspecificallyashing removal of the impurity of an organic system adhering to the vamp surface is carried out by a combustion reaction (C+O*->CO**). Thenplasma treatment is performed in an inert gas atmosphere or a reducing gas atmosphereand sputter etching for defecating the vamp surface is performed like the 1st or 2nd invention. Therebysince impurity removal of an organic system can be performed effectively in addition to natural oxidation film removal on the surface of a vampdefecation on the surface of a vamp can be put into practice more than the 1st and 2nd inventions.
[0025]As a resultlike the 1st and 2nd inventionsreduction of contact resistance of a vamp can be aimed at and high-reliability and high durability can be acquired now in a product assembled by carrying out flip chip mounting.
[0026]
[Embodiment of the Invention]Hereafterit explainsreferring to drawings for the embodiment of this invention. In the complete diagram of an embodimentthe same numerals are given to the portion which is the same or corresponds.
[0027]Firstthe manufacturing method of the solder ball bump by a 1st embodiment of this invention is explained. Drawing 1 is a sectional view for explaining the manufacturing method of the solder ball bump by this 1st embodiment.
[0028]That isin the manufacturing method of this solder ball bumpfirstas shown in drawing 1 Asputtering processthe RIE methodetc. are used for the prescribed position on the semiconductor base substance 1 like the Si wafer in which the circuit element was formedand Al electrode pad 2 of specified shape is formed in it. Nextan opening is formed in the portion corresponding to the Al electrode pad 2 top of this passivation

film after forming a passivation film (not shown) like an SiN film all over this semiconductor base substance 1. Nextan opening is formed in the portion corresponding to the Al electrode pad 2 top of this polyimide film 3 after forming the polyimide film 3 in the whole surface. This polyimide film 3 has a role of the soft error prevention by a surface protectionelectric insulationand alpha rays.

[0029]Nextby patterning mostly this Cr/Cu/Au membrane after identical shape with Al electrode pad 2after laminating a Cr filma Cu filmand Au membrane on the whole surface one by onefor example and forming Cr/Cu/Au membrane in it by sputtering processBLM film 4 which consists of this patterned Cr/Cu/Au membrane is formed. This BLM film 4 also has a role of a barrier metal of the solder ball bump formed behind.

[0030]Nextas shown in drawing 1 Bafter forming a resist film in the whole surfacethis resist film is patterned after specified shape by the lithography method. The numerals 5 show the resist pattern of the specified shape formed by this. This resist pattern 5 has the opening 6 of a predetermined size into the portion corresponding to the BLM film 4 toptherefore the portion corresponding to the Al electrode pad 2 top.

[0031]Nextas shown in drawing 1 Cthe solder film 7 is formed with a vacuum deposition method all over the semiconductor base substance 1. Nextas shown in drawing 1 Da lift off removes the resist pattern 5 with the solder film 7 on it. Therebythe solder film 7 is patterned after desired shape. Nextthe flux (not shown) which uses pitchessuch as an amine system active agentan alcohol solventrosinand polyglycolas the main ingredients is uniformly coated all over the semiconductor base substance 1for example. Thenby heat-treatingusing melting and surface tension of the solder film 7as shown in drawing 1 Ethe almost spherical solder ball bump 8 is formed.

[0032]Thenorganic chemical washing is performed to the semiconductor base substance 1and flux is removed. The numerals 9 show the impurity layer which consists of a contaminant resulting from the natural oxidation film formed in the surface of the solder ball bump 8or a processetc. among drawing 1 E. Herethe impurity layer 9 of the surface of the expedient top of expression and the solder ball bump 8 was exaggeratedand it has written thickly.

[0033]In the manufacturing method of this solder ball bumpas shown in drawing 1 Eafter performing even formation of the solder ball bump 8 by a wetbacksputter etching processing is performed to the semiconductor base substance 1. Herethe case where sputter etching processing is performed as an example using a parallel plate type high frequency plasma processor as shown in drawing 2 is explained. That isas shown in

drawing 2this parallel plate type high frequency plasma processor has the plasma treating chamber 11the positive plate 12and the cathode plate stage 13. The positive plate 12 is grounded and the cathode plate stage 13 is connected with the plasma power source 15 for plasma discharge via the coupling capacitor 14. As this plasma power source 15an RF generator with a frequency of 13.56 MHz is usedfor example. The numerals 16 show the processed board installed on the cathode plate stage 13.

[0034]In this parallel plate type high frequency plasma processorBy introducing process gas and supplying a predetermined plasma discharge output in the plasma treating chamber 11It is possible to perform sputter etching processing of the processed board 16 which made generate the plasma 17 between the positive plate 12 and the cathode plate stage 13and was installed on the cathode plate stage 13 by the ion irradiation from this plasma 17.

[0035]In the manufacturing method of the solder ball bump by this 1st embodiment. After forming the solder ball bump 8 with the semiconductor base substance 1 of the state which shows in drawing 1 Ei.e.a wetbackThe semiconductor base substance 1 in the state where the impurity layer 9 has adhered to the surface of the solder ball bump 8 is introduced into the parallel plate type high frequency plasma processor shown in drawing 2and sputter etching processing is performed in inert gas atmospheressuch as Ar gas.

[0036]Specificallysputter etching processing is performed on the following conditions as an example. That is25sccm and a pressure shall be 1.0 Pastage temperature is made into a room temperature for the flowa plasma discharge output is set to 300W (13.56 MHz)sputter etching processing is performedusing Ar gas as process gasand the processing time is carried out for 60 seconds.

[0037]As shown in drawing 1 Fas a result of this etching process by the sputtering action of Ar^+ ion. While the impurity layer 9 formed in the surface of the solder ball bump 8 is removed effectively and the surface of the pure solder ball bump 8 is exposedthe surface of the polyimide film 3 which is a surface-protection film is chemically activated in response to ion bombardment energy.

[0038]Drawing 3 shows the example which carried out flip chip mounting of the LSI chip which performed above-mentioned sputter etching processing to the printed-circuit board after formation of the solder ball bump 8. In drawing 3the numerals 20 show the passivation film which consists of an SiN film formed on the semiconductor base substance 1. In this casean LSI chip is mounted in a printed-circuit boardas the solder ball bump 8 turns to the bottom. A printed-circuit board consists of the

glass epoxy board 21and the Cu land 22 and the solder resist 23 on this. Where an LSI chip is mounted on a printed-circuit boardalignment of an LSI chip and the printed-circuit board is carried out so that the position corresponding to the solder ball bump 8 may serve as the Cu land 22. These solder ball bumps 8 and the Cu land 22 of each other are connected by the eutectic crystal solder 24. The numerals 25 show the sealing resin which adheres an LSI chip on a printed-circuit board.

[0039]According to this 1st embodimentby performing sputter etching processing to the semiconductor base substance 1 after formation of the solder ball bump 8While the impurity layers 9such as a natural oxidation film of the surface of the solder ball bump 8are removed effectively and the surface of the pure solder ball bump 8 is exposedthe surface of the polyimide film 3 which is a protective film is activated. By thiswhile being able to measure now the electrical property of the solder ball bump 8 correctlyThe product assembled by carrying out flip chip mounting to a printed-circuit board as this device was shown in drawing 3Since both the adhesion strength in the electrical property in the interface of the solder ball bump 8 and the Cu land 22 and the interface of the polyimide film 3 and the sealing resin 25 improvesthe reliability and endurance of a final product are substantially improved compared with the conventional thing.

[0040]Nexta 2nd embodiment of this invention is described. The manufacturing method of the solder ball bump by this 2nd embodiment is the same as that of a 1st embodiment except performing sputter etching processing after solder ball bump formation using the triode type high frequency plasma processor shown in drawing 4.

[0041]Herethe triode type high frequency plasma processor used in this 2nd embodiment is explained first. That isas shown in drawing 4this triode type high frequency plasma processor has the plasma treatment apparatus 31the positive plate 32the lattice electrode 33and the cathode plate stage 34. The positive plate 32 is connected with the plasma power source 36 for plasma production via the coupling capacitor 35and the lattice electrode 33 is grounded. The cathode plate stage 34 is connected with the board bias power supply 38 for board bias via the coupling capacitor 37. As the plasma power source 36an RF generator with a frequency of 2 MHz is usedfor exampleand an RF generator with a frequency of 13.56 MHz is used as the board bias power supply 38for example. A plasma discharge output and substrate bias voltage are independently controlled by these plasma power sources 36 and the board bias power supply 38. The numerals 39 show the processed board installed on the cathode plate stage 34.

[0042]In this triode type high frequency plasma processorIt is possible by introducing process gas and supplying a predetermined plasma discharge output in the plasma treating chamber 31to generate the plasma 40 between the positive plate 32 and the lattice electrode 33and to perform sputter etching processing of the processed board 39 by the ion irradiation from this plasma 40.
[0043]In this 2nd embodimentas shown in drawing 1 Ethe semiconductor base substance 1 after a wetback performs even formation of the solder ball bump 8Sputter etching processing is performed in the atmosphere containing reducing gasintroducing into an above-mentioned triode type high frequency plasma processor as a processed boardand controlling a plasma discharge output and substrate bias voltage independently.
[0044]Specificallysputter etching processing is performed on the conditions shown below as an example. The flow of HF gasusing the mixed gas of HF and Ar as process gas Namely10sccm20sccm and a pressure shall be 1.0 Pastage temperature is made into a room temperature for the flow of Ar gasa plasma discharge output is set to 700W (2 MHz)substrate bias voltage is set to 350V (13.56 MHz)sputter etching processing is performedand the processing time is carried out for 60 seconds.
[0045]According to this 2nd embodimentto the sputtering action of Ar^+ ion in the case of sputter etching processing by in additionthe reducing action by HF. Since the impurity layers 9such as a natural oxidation film of the surface of the solder ball bump 8are removed much more effectivelybeing accompanied by a chemical reactionthe surface of the purer solder ball bump 8 is exposed. The dangling bond of the surface layer of the polyimide film 3 is terminated with a fluoride (F) atom with large electronegativityand will be in a chemical more activity state.
[0046]The product (refer to drawing 3) assembled by carrying out PURIPPU chip mounting of the LSI chip which performed sputter etching processing after solder ball bump formation as mentioned above on a printed-circuit boardThe adhesion strength in the electrical property in the interface of the solder ball bump 8 and the Cu land 22 and the interface of the polyimide film 3 and the sealing resin 25 improves furtherand the final reliability and endurance of a product are substantially improved like the case of a 1st embodiment compared with the former.
[0047]Nexta 3rd embodiment of this invention is described. The manufacturing method of the solder ball bump by this 3rd embodiment is the same as that of a 1st embodiment except performing ashing treatment and sputter etching processing after solder ball bump formation using the ICP high-density-plasma processing unit shown in drawing 5.

[0048]Herethe ICP high-density-plasma processing unit used in this 3rd embodiment is explained first. That isas shown in drawing 5this ICP high-density-plasma processing unit has the plasma treating chamber 41the inductive coupling coil 42and the stage 43. The joint induction coil 42 is connected with the ICP power supply 44 for plasma dischargeand the stage 43 is connected with the board bias power supply 46 for board bias via the coupling capacitor 45. As the ICP power supply 44an RF generator with a frequency of 450 kHz is used and an RF generator with a frequency of 13.56 MHz is used as the board bias power supply 46. A plasma discharge output (ICP source mode output) and substrate bias voltage are independently controlled by these ICP power supplies 44 and the board bias power supply 46. The numerals 47 show the processed board installed on the stage 43. Herethe stage 43 is perpendicularly (direction shown by an arrow among drawing 5) movable.
[0049]In this ICP high-density-plasma processing unitIt is possible by introducing process gas and supplying a predetermined ICP source mode output in the plasma treating chamber 41to perform plasma treatment by the plasma 48 as for which more than 1x10 $^{11}cm^{-3}$ has the density of less than 1x10 $^{14}cm^{-3}$for example.
[0050]In this 3rd embodimentas shown in drawing 1 Ethe semiconductor base substance 1 after a wetback performs even formation of the solder ball bump 8After performing ashing treatment in the atmosphere containing oxygenintroducing into an above-mentioned ICP high-density-plasma processing unit as a processed boardand controlling independently an ICP source mode output and substrate bias voltagesputter etching processing is continuously performed in the atmosphere containing reducing gas.
[0051]Specificallyashing treatment is first performed on the conditions shown below as an example. The flow of O_2using oxygen (O_2) as process gas Namely100sccmA pressure shall be 1.0 Pastage temperature is made into a room temperatureICP source power is set to 1000W (450 kHz)substrate bias voltage is set to 0V (13.56 MHz)ashing treatment is performedand the processing time is made into 10 seconds.
[0052]Nextconditions are switched as follows as an example and sputter etching processing is performed. The flow of HF gasusing the mixed gas of HF and Ar as process gas Namely10sccm20sccm and a pressure shall be 0.2 Pastage temperature is made into a room temperature for the flow of Ar gasICP source power is set to 1000W (450 kHz)substrate bias voltage is set to 100V (13.56 MHz)sputter etching processing is performedand the processing time is made into 10 seconds.
[0053]According to this 3rd embodimentthe surface layer of the polyimide

film 3 which is a protective film of a device serves as the form where O atom was incorporated during that combinationby it at the same time the impurity of an organic system which adhered to the surface according to a process reason is effectively removed by ashing treatment by a combustion reaction.

[0054]And while the impurity layers 9such as a natural oxidation film of the surface of the solder ball bump 8are accompanied by a chemical reaction by the reducing action by HFweld slag removal is effectively carried out by the sputter etching processing performed succeeding thisand the surface of the purer solder ball bump 8 is exposed by it. The outermost superficial layer of the polyimide film 3 is terminated by F atom (it containsalso when O atom introduced at the time of ashing treatment is replaced by F atom)and will be in a chemical still activity state.

[0055]The product (refer to drawing 3) assembled by carrying out PURIPPU chip mounting of the LSI chip which performed sputter etching processing after solder ball bump formation as mentioned above on a printed-circuit boardThe adhesion strength in the electrical property in the interface of the solder ball bump 8 and the Cu land 22 and the interface of the polyimide film 3 and the sealing resin 25 improves furtherand the final reliability and endurance of a product are substantially improved like the case of 1st and 2nd embodiments compared with the former.

[0056]When performing the ashing treatment and sputter etching processing which are performed after formation of the solder ball bump 8 according to this 3rd embodimentUsing an ICP plasma sourceon high-density plasma and a concrete target. For examplewith more than $1x10^{11}cm^{-3}$ processing with the plasma density of less than $1x10^{14}cm^{-3}$ by thisIt comes to enter into the semiconductor base substance 1 verticallywithout scattering about the ionic species generated so much when the processing under low-pressure power atmosphere was attained. for this reasonthe surface treatment (ashing treatment and sputter etching processing) of the semiconductor base substance 1 after the bump formation by ion irradiation -- a high speed -- and it is efficiently realizable.

[0057]Since it is possible to control independently the ion energy which enters into the semiconductor base substance 1 from plasmawithout affecting the creation state of plasmaShortening of processing time can be aimed at also on the conditions which set up substrate bias voltage low in consideration of the process damage to a devicewithout causing the fall of processing speed.

[0058]Although the embodiment of this invention was described concretely

abovethis invention is not limited to an above-mentioned embodimentand it cannot be overemphasized that it is selectable suitably in the range which does not deviate from the main point of an inventionsuch as sample structurea process unitand a process condition.
[0059]For examplealthough the above-mentioned 1st - a 3rd embodiment showed the case where the lift off of membrane formation by vacuum deposition and a resist pattern was used as a pattern formation method of a solder ball bumpapplication to the manufacturing method using the other electrolytic plating etc. is also possible.
[0060]Although 2nd and 3rd embodiments showed the example which used HF as gas of reduction naturehydrogen (H_2)chloride (HCl)etc. can also be similarly used in addition to it. Among thesewhen using liquid sourcessuch as HF and HClit introduces in a process chamber with techniquessuch as bubbling by carrier gassuch as helium (helium)heating evaporationand ultrasonic evaporation.
[0061]
[Effect of the Invention]As explained aboveaccording to this inventionthe natural oxidation film and process residue which were formed on the surface of the vamp can be removed effectivelyand the surface of a pure vamp can be exposed. as a resultthe electrical property of the device which produced the vamp improves -- having (contact resistance decreases) -- the reliability and endurance of the product assembled by carrying out PURIPPU chip mounting can be substantially raised now compared with the former.
[0062]Thereforethis invention is very effective in manufacture of the semiconductor device of which it is designed based on a detailed design ruleand the degree of high integrationhigh performanceand high-reliability are required.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a sectional view for explaining the manufacturing method of the solder ball bump by a 1st embodiment of this invention.
[Drawing 2]It is an approximate line figure showing an example of the parallel plate type high frequency plasma processor used in the manufacturing method of the solder ball bump by a 1st embodiment of this invention.
[Drawing 3]It is an approximate line figure showing the example which carried out flip chip mounting of the LSI chip which performed sputter

etching processing after solder ball bump formation to the printed-circuit board.

[Drawing 4]It is an approximate line figure showing an example of the triode type high frequency plasma processor used in the manufacturing method of the solder ball bump by a 2nd embodiment of this invention.

[Drawing 5]It is an approximate line figure showing an example of the ICP high-density-plasma processing unit used in the manufacturing method of the solder ball bump by a 3rd embodiment of this invention.

[Drawing 6]It is a sectional view for explaining the manufacturing method of the conventional solder ball bump.

[Drawing 7]It is an approximate line figure for explaining the situation of measurement of the electrical property of a solder ball bump.

[Description of Notations]

1 [... A BLM film5 / ... A resist pattern6 / ... An opening7 / ... A solder film8 / ... A solder ball bump9 / ... An impurity layer22 / ... Cu land25 / ... Sealing resin] ... A semiconductor base substance2 ... An Al electrode pad3 ... A polyimide film4